IN THE CLAIMS

Please amend claims as follows:

1. (Currently Amended) A system comprising:

an execution pipeline;

a power delivery unit to provide power to the execution pipeline at a specified operating point, wherein the power delivery unit includes a clock gating circuit to control power delivery to one or more units of the execution pipeline, the clock gating circuit including a plurality of gating units that each control a clock signal to an associated unit in the execution pipeline and provide a signal indicative of the activity state of the associated unit that is being monitored for power consumption;

a digital throttle to estimate a power state, responsive to activity of the execution pipeline and the specified operating point, and to trigger a change in the operating point, responsive to the estimated power state reaching a first threshold.

2. (Cancelled)

3. (Previously Presented) The system of claim 1, wherein the digital throttle comprises an activity monitor to estimate an activity level responsive to a signal from the clock gating circuit, the activity monitor including a scaling unit to adjust the estimated activity level, responsive to the current operating point.

4. (Original) The system of claim 3, wherein the scaling unit includes:

a look-up table to store scaling factors for a plurality of operating points; and

a multiplier to multiply the estimated activity level by the scaling factor associated with the current operating point.

5. (Original) The system of claim 3, wherein the monitor unit further comprises:

a plurality of weight units, each weight unit being associated with one of the units of the execution pipeline; and

an adder to receive a first or second value from each weight unit, responsive to the signal from the clock gating circuit.

6. (Cancelled)

7. (Previously Presented) The system of claim 3, wherein the activity monitor includes:

a look-up table to store scaling factors corresponding to a plurality of operating points; and

a scaling unit to adjust the activity level according to a scaling factor appropriate for the specified operating point.

8. (Original) The system of claim 7, further comprising a conversion circuit to determine a power state from the adjusted activity level.

9. (Original) The system of claim 8, wherein the conversion circuit compares the adjusted activity level with a threshold level and stores the difference in an accumulator.

10. (Original) The system of claim 9, wherein the conversion unit scales the threshold level responsive to the current operating point.

11. (Currently Amended) A processor comprising:

an execution pipeline;

a clock gating circuit to control power delivery to one or more units of the execution pipeline, including the clock gating circuit including a plurality of gating units that each control a clock signal to an associated unit in the execution pipeline and provide a signal indicative of the activity state of the associated unit that is being monitored for power consumption;

a monitor unit to estimate an activity level of the execution pipeline, responsive to ~~a status~~ signals from the gating units of the clock gating circuit;

a scaling unit to adjust the estimated activity level, responsive to an operating point of the processor; and

a threshold comparator to determine if the scaled, estimated activity level meets a first threshold level.

12. (Original) The processor of claim 11, wherein the scaling unit includes a look-up table and a multiplier, the look-up table to provide a scale factor to the multiplier, responsive to the operating point of the processor.

13. (Original) The processor of claim 12, wherein the operating point of the processor is specified by a voltage and a frequency.

14. (Original) The processor of claim 11, further comprising an accumulator to increment a stored value by a difference between the scaled, estimated activity and the first threshold if the scaled activity exceeds the first threshold.

15. (Original) The processor of claim 14, further comprising a comparator to compare the stored value with a second threshold and to assert a power-reduction signal if the stored value reaches the second threshold value.

16. (Original) The processor of claim 11, wherein the activity monitor includes an adder having one or more weighted inputs, each input associated with the one or more pipeline units, respectively.

17. (Original) The processor of claim 16, wherein the status signal comprises one or more status signals associated with the one or more pipeline units, respectively.

18. (Original) The processor of claim 17, wherein the adder sums a first or a second value from each of the weighted inputs, responsive to a state of the associated status signal.

19. (Currently Amended) A method for controlling power consumption in a processor comprising:

monitoring activity states for pipeline units of the processor <u>using signals from individual gating units that are each associated with a pipeline unit that has its power</u>

consumption level being monitored, wherein each gate unit controls a clock signal to activate its associated pipeline unit as it is needed;

estimating a power state for the processor using the monitored activity states and an operating point of the processor;

comparing the estimated power state with a threshold value; and

adjusting the operating point of the processor if the estimated power state exceeds the threshold value.

20. (Original) The method of claim 19, wherein estimating the power state comprises:

determining an activity level from the monitored activity states;

scaling the activity level according to the operating point;

normalizing the scaled activity level relative to a first threshold; and

accumulating the normalized, scaled activity level for a series of clock intervals.

21. (Original) The method of claim 19, wherein monitoring activity states comprises monitoring status signals provided by gate units associated with the pipeline units of the processor.

22. (Cancelled)

23. (Previously Presented) The method of claim 19, wherein adjusting the operating point of the processor comprises adjusting a frequency of the clock signal.

24. (Original) The method of claim 23, wherein adjusting the operating point further comprises adjusting a voltage of the clock signal.

25. (Original) The method of claim 19, wherein estimating the activity level comprises:

adding a first or a second weight value to a sum, responsive to a pipeline unit being in a first or a second activity state, respectively; and

scaling the sum by a factor associated with the current operating point.

26. (Previously Presented) The method of claim 25, wherein estimating the activity level further comprises adding a weight to the sum to represent pipeline units that operate in a single activity state.

27. (Currently Amended) A computer system comprising:

a memory system to store instructions for execution;

an instruction execution pipeline including a plurality of units to execute the instructions;

a power delivery system to deliver power to the execution pipeline at a current operating point, the power delivery system includes plural gate units to control power delivery to one or more units of the execution pipeline and to provide signals indicative of the activity state of associated units of the execution pipeline that are having their power consumption level monitored;

an activity monitor to estimate an activity level for the execution pipeline at the current operating point using signals from the plural gate units; and

a throttle circuit to adjust the current operating point, responsive to a power state determined from the activity level falling outside a specified range.

28. (Previously Presented) The computer system of claim 27, wherein each gate unit indicates a first or second activity state for a unit of the execution pipeline, according to the unit's being active or inactive in a clock interval.

29. (Original) The computer system of claim 28, wherein activity monitor includes an adder to add a first or a second weight to the activity level, responsive to the gate unit indicating a first or second state for its associated pipeline unit in the clock interval.

30. (Original) The system of claim 29, wherein the activity monitor further includes a scale unit to scale the activity level for the clock interval according to the current operating point of the processor.